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Design Note 15

7768 4K RAM BOARD

1. Introduction

This board provides a 4096 word, 8 bit, Random Access Memory for use with the 7768 or any similar CPU. The board size, electrical characteristics and pin connections are compatible with the 7768 CPU bus structure.

For those with shallow pockets, the board can be initially equipped for only 1024 words, and subsequentally expanded in 1024 (1K) word increments.

Multiple 4K RAM boards may be fitted to a system up to a maximum of 16 boards (64K words of memory). Address selection straps on the board can be set to ensure that the particular board responds only to addresses within a particular 4K address block.

2. Board Characteristics

Capacity	1024 (1k) 8 bit words minimum 4096 (4K) 8 bit words maximum
Bus	Fully buffered on all lines. Compatible with 7768 CPU.
Speed	Depends upon type of memory IC fitted
Power	Requires +5V stabilised DC @ 1.1A typical, 1.8A worst case using standard 2102 or 2102-1 memory IC's. 1.1A worst case if low power versions (2102 L) fitted.
Construction	8.0"x8.0" single sided PCB with gold plated 0.1" spacing edge connector

3. Circuit Description

The heart of the board is the array of memory IC's X8-39. Each of these IC's contains 1024 bistables, each capable of storing one bit of information, thus the total information which can be stored on the board is 32 x 1024 bits, organised as 4096 x 8 bit words.

The least significant ten lines of the address bus (A0-A9) are buffered by X6, X7 and then fed to all memory IC's to select the required bit from the 1024 (1024 = total number of possible combinations of the 10 binary address line states) stored in each IC. The inversion of A0-9 caused by X6, 7 is irrelevant; it just means that an individual bit of information is stored in a different place inside the memory IC, but as the invertion happens during a 'read' operation as well as during a 'write', the correct information is retrieved.

The next two most significant address lines, A10 and A11, are fed to one out of four decoder X5 and cause one of its outputs to go to logic 0 (low, the other three outputs being at logic 1. These four outputs are connected to the 'chip enable' inputs of the four banks of memory IC's to select one bank at a time according to the state of A10, A11;

A10	A11	Mem IC's selected
0	0	X8-11, 24-27
0	1	X16-19, 32-35
1	0	X12-15, 28-31
1	1	X20-23, 36-39

Each memory IC has one pin for data input, which is fed from the appropriate line of the data bus D0-D7 via the permanently enabled data input buffers (part of X1, 2). A data out pin is also provided on each memory IC, and this is a tri-state output, active only when the chip's CE input is low. The outputs of the corresponding memory IC's in each bank may therefore be connected together and to the inputs of the data output buffers (part of X1, 2).

The four most significant address lines A12-A15 are passed via Exclusive or gates (X4) to the Nand gate X3. The other inputs of the X4 gates may be strapped to either logic 0 (ground) or to logic 1 (+5v via protective resistor R1). According to the setting of the strap the Exclusive or gate will either invert the signal on the address line (other input strapped to 1) or pass it unaltered (other gate input strapped to 0). Thus by suitable strapping the memory card can be made to respond to any one of the 16 4K memory address blocks within the 7768 CPU's addressing capability.

When A12-15 are in the correct state (address present on the address bus lines within the 4K block selected for the board), X3 goes low, enabling the second half of the dual one out of four decoder X5. The other two inputs of this half of X5 are connected to the system control bus lines R/W ('1' for a read, '0' for write) and E (enable) such that;

- during a READ operation, the card output buffers (part of X1, 2) are enabled when E = 1, to feed the selected data onto the system data bus lines D0-8.
- during a WRITE operation the memory IC R/W inputs are set to '0' (=write) when E=1, thus storing the information present on the data bus at that time into the correct location in memory.

4. Construction

Refer to figs 2, 3, 4.

Because of the complexity of the unit, and the need for careful layout to minimise the effects of transient current spikes, it is recommended that the printed circuit board available from BMS is used.

The close spacing of the tracks on this board means that great care has to be taken to avoid accidental shorts between tracks due to, for example, solder splashes. The constructor should therefore take care to make good soldered joints using the minimum amount of solder whilst ensuring that a joint is made all round the component pin or wire end. Use of a small soldering iron with a small, clean bit is essential. Also, before fitting any component, feel all over the track side of the board for any loose copper swarf left from the board drilling process, and examine it carefully for unetched copper 'bridges' between tracks.

The use (or not) of IC sockets is largely a matter for personal preference. Poor quality sockets must be avoided as they can cause many hard to trace faults. Provided that the constructor is sure of the quality of the IC's he is using, is confident of his ability to solder them in the right way round first time, and is using a low leakage soldering iron, then there is no reason why all of the IC's should not be soldered directly into the board. In case of trouble the author's favourite method of removing a suspect IC is to first cut the body of the IC free from all leads, then to unsolder and extract the leads one at a time. This procedure ruins the suspect IC, but does least damage to the board.

The best order of construction is;

First fit all the straps (not the ribbon cables at this stage) using sleeved wire where appropriate. One way of obtaining thin sleeved wire is to take a length of thin single solid cored insulated wire, strip off the insulation for about ½" at each end, then, grasping the inner wire firmly at each end with two pairs of pliers (or one pair and a vice), pull until you can feel the copper wire stretch and flow.

This operation reduces the diameter of the wire slightly so that it will slide freely within the insulation, and it also removes the 'spring' from the wire so that it may be formed more easily. Note that some straps on this board require the use of a thin wire so that two ends may be inserted into a single hole.

Next, form and fit the ribbon cables as shown in Figs 2 & 3, followed by the IC's and finally R1 and C1-21.

If the board is to be only partially equipped, fit the memory IC's in the following order;

First	X8-11, 24-27	(address range X000-X3FF)
Next	X12-15, 28-31	(" " X400-X7FF)
Then	X16-19, 32-35	(" " X800-XBFF)
Finally	X20-23, 36-39	(" " XC00-XFFF)

Where X is determined by the strapping of X4 inputs.

After assembly clean the track side of the board thoroughly with a small stiff brush (a very hard toothbrush is ideal) and examine it carefully for short circuits caused by bent leads, excess solder on joints, solder splashes etc.

5. Testing

a) Check carefully with an ohm-meter for short circuits between tracks connecting X8-39, also between OV and +5v lines. (note that some reading is to be expected due to the internal resistances of the IC's). This stage is most important as it can reveal faults which would otherwise be extremely difficult to locate.

b) Strap pins 1, 13, 4, 10 of X4 so that the board will respond to the desired address range. (The first memory board in a system should be set to the lowest address block; 0000 to 0FFF).

c) Make sure that all used pins on the RAM board are correctly wired to the corresponding pins on the CPU board socket.

d. If the system only consists of the CPU plus this memory, then connect pin 5 of the CPU board (256SEL) to pin 36 (A15). This will ensure that the 256 word memory on the CPU card responds only to addresses above 8000, and will therefore not interfere with the memory board. If a monitor card is included with the system then proceed to step E.

Check that the CPU board still works by loading and running the following program;

Address	Code		
FF00	08	START:	INX
FF01	26 FD		BNE Start
FF03	4C		INC A
FF04	B7 FF FF		STA A Display
FF07	20 F7		BRA Start
FFFE	FF		start address

This is a Verson 1 Flasher (from the CPU manual) modified to operate in high memory. It increments the display about once a second. Note that the high 8 bits of the address (FF in each case) are shown for completeness, but are not set up by the user when loading the program via the control panels switches, the load logic on the CPU card automatically forces the high order address lines to FF during a manual load operation. Note also the need to load the high order byte of the Reset vector (into address FFFE) to ensure that the program is started at the correct location (FF00), and the need to use the full (extended) address (FFFE) of the display in the STA instruction. Running this program will check that the CPU card, and the 256 word memory on it, still works.

e) Now switch off, plug in the memory card and, carefully monitoring the +5V supply, switch back on.

Leave the equipment on for a few minutes while checking for signs of overheating of any component. Then check that the rest of the system still works correctly; by testing the operating system if a monitor card is fitted, or by the program given above if only the 'bare bones' CPU is available.

f) Finally, run one of the memory test routines given in the appendices and, if all is well, leave the routine running for several hours to pick up any early life failures. It is also work tapping all over the board (with the end of a pencil) while the test routine is running to reveal dry joints.

6. Diagnostics

To be performed with the board removed from the system and supplied with 5V DC.

Test signals to be applied to connector;

'0' = direct connection to 0V
'1' = connection to +5V via 1K resistor.

Measurements made with 20K/V or better meter;

'0' - 0 to 0.4V
'1' = +2.4 to +5v anything in between is wrong

a) Address Buffers X6, 7

Output of inverter should be opposite to input;

Check that X7 pin 6 is '1' when '0' applied to pin 21 (A0)
X7 pin 6 is '0' when '1' applied to pin 21 (A0)
X7 pin 4 is '1' when '0' applied to pin 22 (A1) etc

b) Exclusive or gates X4

With A. B. C. D all connected to R1;

Check that X4 pin 3 is '1' when '0' is applied to pin 22 (A12)
X4 pin 3 is '0' when '1' is applied to pin 33 (A12) etc

c) Nand gate X3

With X4 outputs (pins 3, 11, 6, 8) at '1' (by strapping A.B.C.D. to R1 and applying '0' to A12-A15) X3 pin 8 should be 0.

d) ½ Decoders X5

Check the outputs on pins 4, 5, 6, 7 of X5 for different conditions applied to A10, A11;

Inputs		X5 output pins
A11	A10	4 5 6 7
0	0	0 1 1 1
0	1	1 0 1 1
1	0	1 1 0 1
1	1	1 1 1 0

With X3 pin 8 set to 0 (as (c) above check X5 pins 9 & 10 for different combinations of inputs R/W and E;

Inputs		X5 outputs pins
E	R/W	10 9
0	0	1 1
0	1	1 1
1	0	0 1
1	1	1 0

e) Input data buffers (part of X1, 2)

Apply '0' to E input to card, then check that;

X1 pin 17 is '0' when '0' applied at D0
X1 pin 17 is '1' when '1' applied at D0 etc

f) Output data buffers (part of X1, 2)

Check that the buffer outputs can be set to the high impedance state by applying '0' to card E input then checking each data bus line D0-D7 as follows;

- temporarily connect data line to OV via 1K resistor, voltage across resistor should be less than 0.1V.
- temporarily connect data line to +5V via 1K resistor, voltage across resistor should be less than 0.1V.

Then set A12-A15, E & R/W inputs to cause X5 pin 9 to go to 0 (as (D) above to enable output buffers, and check that the output of each buffer (X1 & 2 pins 3, 5, 7, 9) is the same as that present on their inputs (X1, 2 pins 2, 4, 6, 8). Note that the signal present on the input of each data output buffer is coming from memory, which will be holding a random pattern, and by trying different logic inputs to A0-A11 card inputs it should be possible to find a memory cell containing a '1', and another which will give a '0' output thus testing both states of the output buffer.

g) Memory IC's X8-39

Faults on these are best detected by use of one of the test programs given in the appendices.

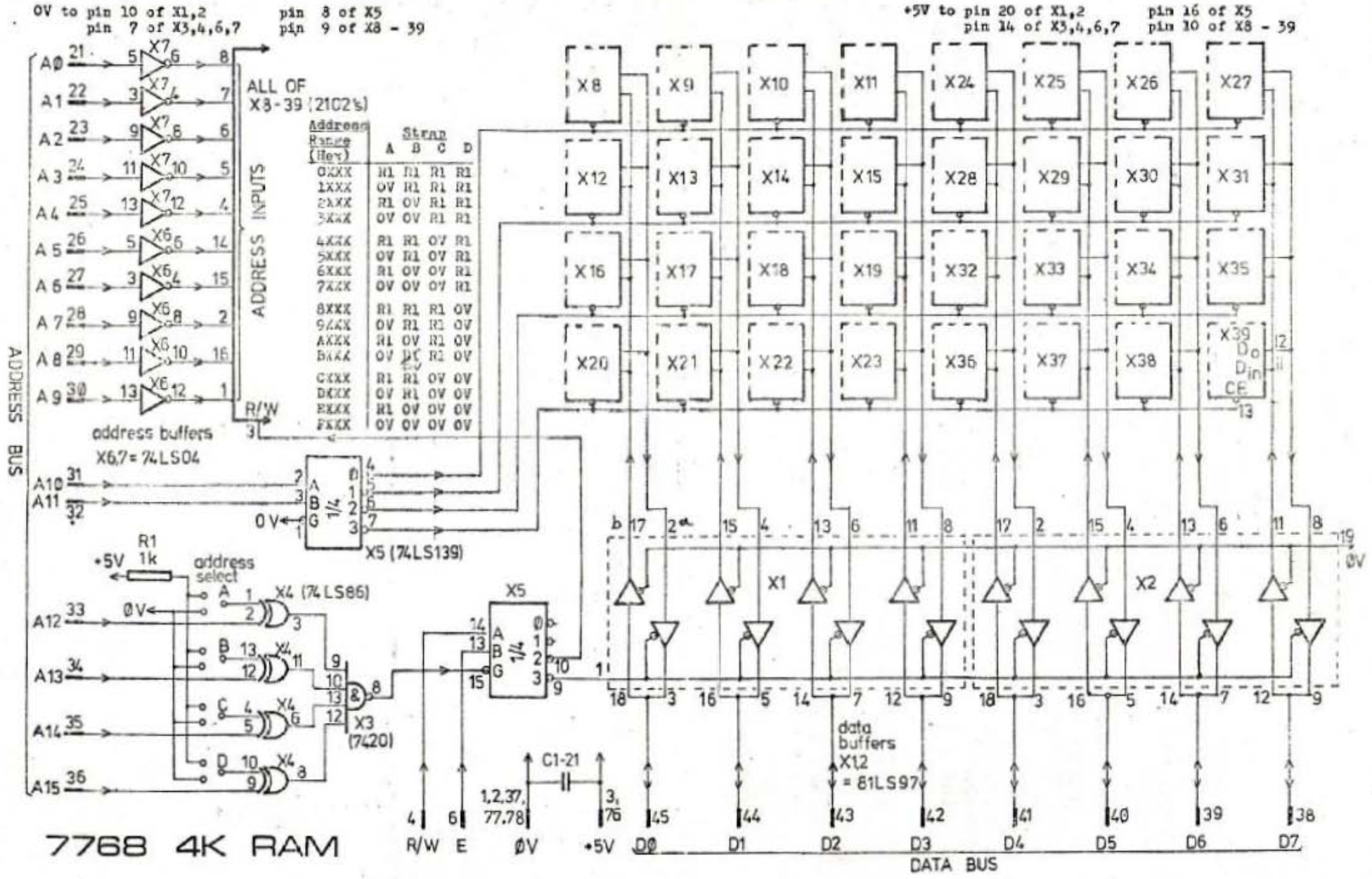
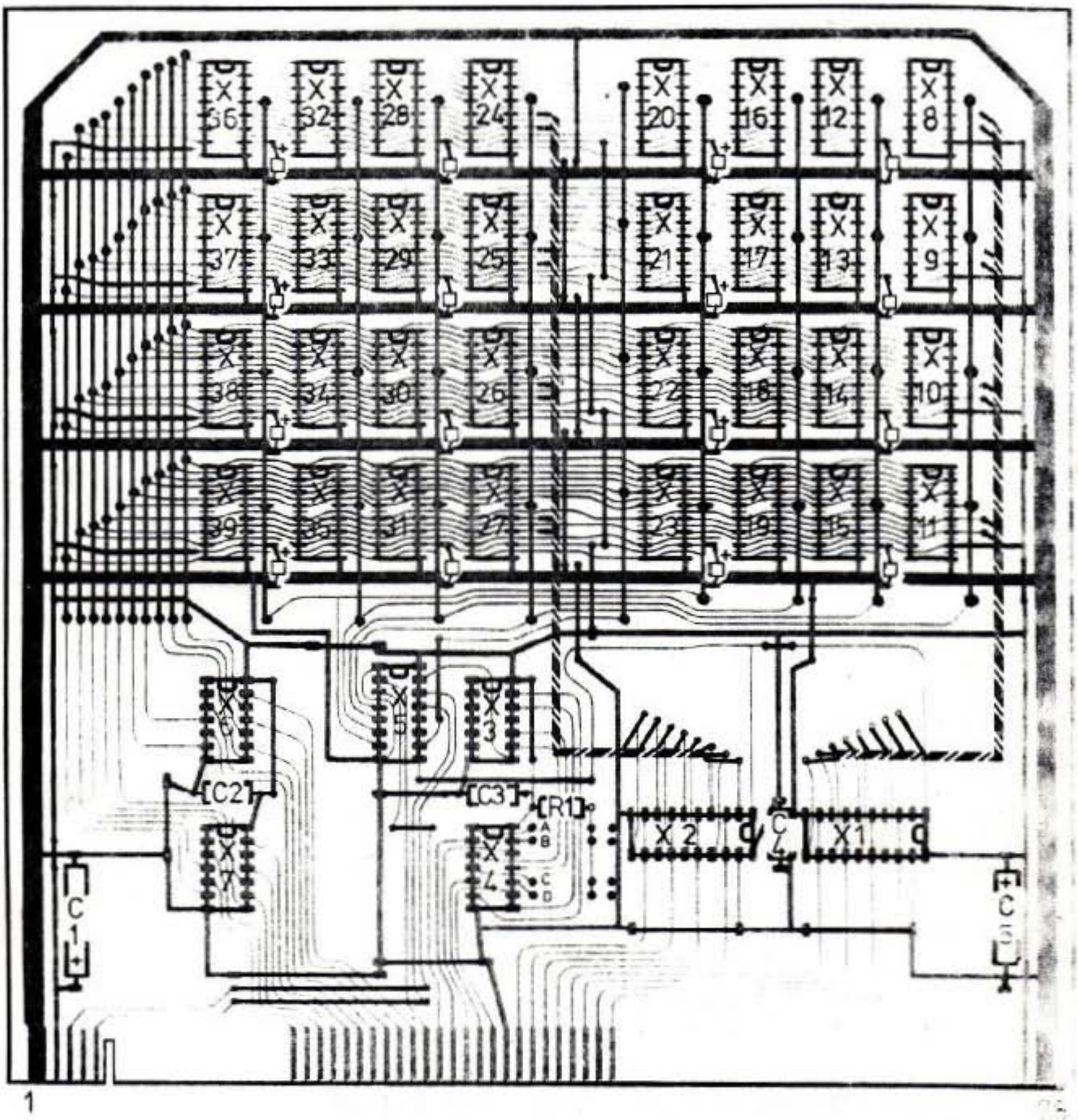

0V to pin 10 of X1,2
pin 7 of X3,4,6,7
pin 8 of X5
pin 9 of X8 - 39
+5V to pin 20 of X1,2
pin 14 of X3,4,6,7
pin 16 of X5
pin 10 of X8 - 39
ALL OF X8-39 (2102's)
ADDRESS INPUTS
ADDRESS BUS
address buffers X6,7 = 74LS04
R/W
X5 (74LS139)
R1 1k
+5V
address select
X4 (74LS86)
X3 (7420)
C1-21
data buffers X1,2 = 81LS97
X1
X2
X8
X9
X10
X11
X24
X25
X26
X27
X12
X13
X14
X15
X28
X29
X30
X31
X16
X17
X18
X19
X32
X33
X34
X35
X20
X21
X22
X23
X36
X37
X38
X39
Do
Din
CE
7768 4K RAM
R/W
E
0V
+5V
D0
D1
D2
D3
D4
D5
D6
D7
DATA BUS

Fig 1



1

7768 4K RAM BOARD
component side view

Notes;

Strap on component side of board, linking 2 pcns

" " " " " " " >2 pcns

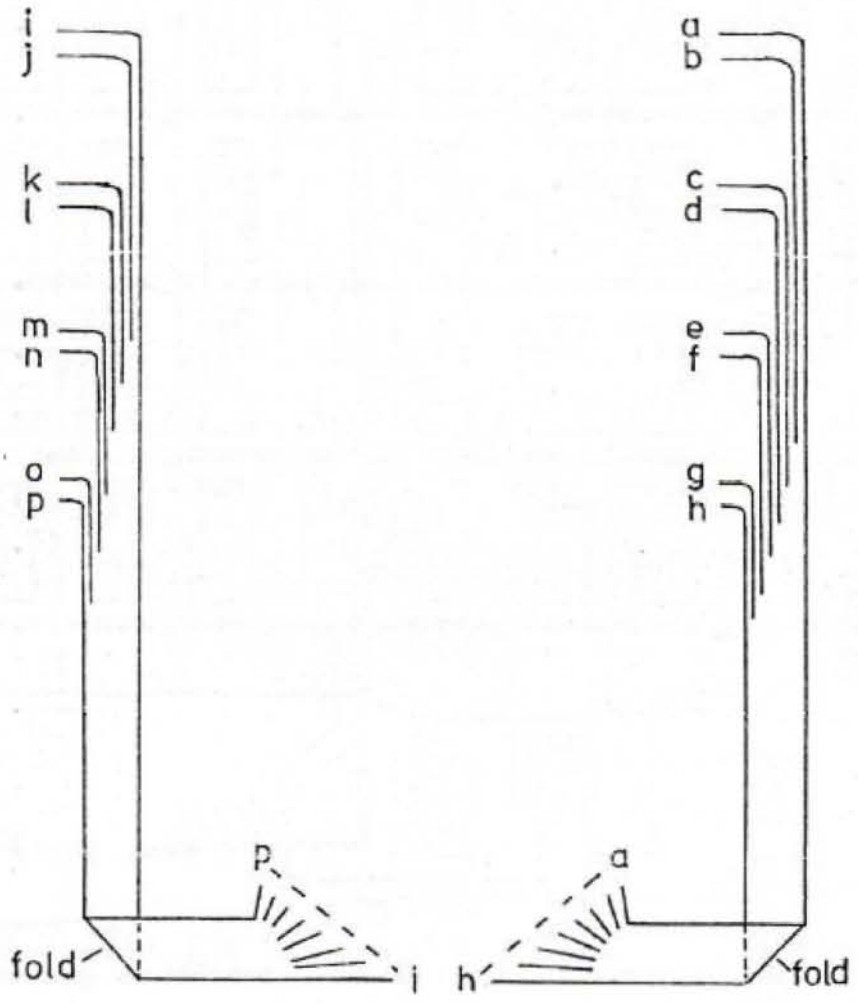
Ribbon cable

C6-13

C14-21

See text for connections to ABCD

Fig. 2



7768 4K RAM BOARD

Arrangement of ribbon cables - not to scale.

Use solid cored type , e.g. Doram's miniature cable No. 357-491.

Fig. 3

7768 4K RAM BOARD

Components

Logic

X1, 2	81LS97	Octal Tri-state Buffer
X3	7420	Dual 41/P Nand gate
X4	74LS86	Quad Exclusive or gate
X5	74LS139	Dual ½ Decoder
X6, 7	74LS04	Hex Inverter
X8-39	2102	1024x1 static ram - for 1.6us CPU Board
or	2102-1	- for 1.2us CPU Board

Resistor

R1	1K ¼ watt

Capacitors

C1, 5	33uf 10v or similar small electrolytic
C2, 3, 4	0.1uf
C6-13	6.8uf 10v or similar tantalum bead
C14-21	0.047uf 12v small disc ceramic

Misc.

32 off	16 pin DIL sockets
Ribbon cable	Miniature solid cored type
Printed circuit	board
Edge connector	77 way + polarising key, 0.1" single sided

Fig 4

Appendix 1

MEMTEST Ø1

Memory Test Program for use with 'Bare Bones' system (CPU & MEM boards only, 1/O via control panel data switches & lamps).

See attached listing.

This program first loads all specified memory locations with (different) patterns, then reads the contents of each memory location, checking it against the stored pattern. If all is well, the control panel data display is incremented (to assure the user that something is happening) then the process is repeated with a slightly different set of patterns.

It at any stage the pattern read from a memory location differs from that written in, the program will store;

- the address of the faulty memory location in FF50 (high byte) and FF51 (low byte).
- the pattern expected, in memory location FF52.
- the pattern actually read, in memory location FF53.

The program will then stop, thus turning off the 'RUN' lamp to alert the user, who can then use the control panel to read the information about the fault from locations FF50-FF53.

As shown, the program will test memory from 0000 to OFFF (Lowest 4k bytes of memory address space. Change locations FF54 - FF57 to examine a different area.

To test that the program is working, one can short (with the blade of a small screwdriver) between pins 15 & 16 on one of the memory IC's to simulate an addressing failure.

The test patterns are generated by adding the contents of the 6800 accumulator B to the pattern written into the previous address. When all specified memory locations have been written into and checked, accumulator B is incremented so that next time round a different set of patterns will be generated.

BEAR MICROCOMPUTER SYSTEMS
24 College Road, Maidenhead, Berks, SL6 6BN

HEXADECIMAL CODING FORM

PROGRAM MEMTEST01	VERSION 1	AUTHOR MRL	DATE 4/11/77	PAGE 1 OF 1

ADDRESS	MACHINE CODE	LABEL	OPERATOR & OPERAND	COMMENTS
FF00	FE FF 54	START	LDX LOMEM	POINT @ START OF MEMORY UNDER TEST
FF03	4F		CLR A	
FF04	1B	LOOP1	ABA	GENERATE PATTERN
FF05	A7 00		STA A 00,X	WRITE PATTERN
FF07	08		INX	POINT @ NEXT MEMORY LOCATION
FF08	BC FF 56		CPX HIMEM	END OF MEM TEST AREA ?
FF0B	26 F7		BNE LOOP1	
FF0D	FE FF 54		LDX LOMEM	PREPARE TO CHECK MEMORY CONTENTS
FF10	4F		CLR A	
FF11	1B	LOOP2	ABA	GENERATE PATTERN AGAIN
FF12	A1 00		CMP A 00,X	STORED INFORMATION OK ?
FF14	26 0C		BNE FOLT	
FF16	08		INX	POINT @ NEXT LOCATION
FF17	BC FF 56		CPX HIMEM	ALL CHECKED ?
FF1A	26 F5		BNE LOOP2	
FF1C	5C		INC B	SET UP FOR NEW PATTERN SEQUENCE
FF1D	F7 FF FF		STA B DISPLAY	RE-ASSURE OPERATOR Display FOFF
FF20	20 DE		BRA START	& CHECK MEMORY AREA AGAIN
FF22	FF FF 50	FOLT	STX ADDR	STORE ADDRESS OF FAULT
FF25	B7 FF 52		STA RIGHT	& BYTE WRITTEN
FF28	A6 00		LDA 00,X	
FF2A	B7 FF 53		STA WRONG	& BYTE READ
FF2D	8E FF 4F		LDS #TMPSTK	PREPARE FOR 'WAI'
FF30	3E		WAI	TURN OFF 'RUN' LAMP
FF4F	00	TMPSTK		PLACE TO PUT STACK FOR 'WAI'
FF50	00 00	ADDR		ADDRESS OF FAULT WILL BE STORED IN THESE TWO BYTES.
FF52	00	RIGHT		INF THAT WAS WRITTEN WILL BE STORED HERE.
FF53	00	WRONG		INF THAT WAS READ WILL BE STORED HERE
FF54	00 00	LOMEM	#0000	ADDRESS OF LOW END OF MEMORY AREA UNDER TEST
FF56	10 00	HIMEM	#1000	ADDRESS OF HIGH END OF MEMORY AREA UNDER TEST PLUS 1
FFFE	FF	RVECT		HIGH BYTE OF RESET VECTOR